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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rong LIN — Group Art Unit: 2124

Serial No.: 10/728,485 — Docket: 1181-23

Filed: December 5, 2003 — Dated: June 27, 2005

For: UNIFIED MULTIPLIER TRIPLE-EXPANSION SCHEME AND EXTRA REGULAR COMPACT LOW-POWER IMPLEMENTATIONS WITH BORROW PARALLEL COUNTER CIRCUITS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to Applicant's duty of disclosure, the information listed in the attached form PTO-1449 is brought to the attention of the Examiner. A copy of each reference is attached hereto.

The citation of the listed items is not a representation that they constitute a complete or exhaustive listing of the relevant art or that the references are prior art. The items listed are submitted in good faith, but are not intended to substitute for the Examiner's search. It is hoped, however, that in addition to apprising the Examiner of these particular items, they will assist in identifying fields of search and in making as full and complete a search as possible.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postpaid in an envelope, addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 27, 2005.

Dated: June 27, 2005

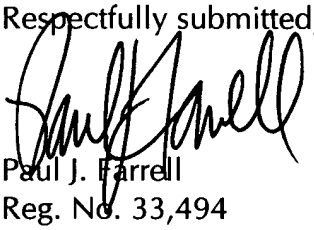
Paul J. Farrell

The filing of this Information Disclosure Statement is not an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

To the best of Applicant's knowledge, this Information Disclosure Statement is being filed before the date of mailing of a first Office Action in connection with this case.

The claims of the application as now presented are believed to patentably distinguish over the prior art and to be in condition for allowance. Early and favorable consideration of the case is respectfully requested.

Respectfully submitted,



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Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 1181-23	SERIAL NO. 10/728,485
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	APPLICANT Rong LIN	
	FILING DATE December 5, 2003	GROUP ART UNIT 2124

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		1.	A. D. Booth, A Signed Binary Multiplication Technique, The Quarterly Journal of Mechanics and Applied Mathematics, Vol. 4, Part 2, June 1951, pp. 236-238.
		2.	C. S. Wallace, A Suggestion For A Fast Multiplier, IEEE Transactions on Electronic Computers, Vol. Ec-13, 1964, pp. 14-17
		3.	Itoh et al., A 600MHz, 54 x 54-bit Multiplier With Rectangular-Styled Wallace Tree, IEEE Journal of Solid-State Circuits, Vol. 36, No. 2, February 2001, pp. 249-257.
		4.	Montoye et al., A Double Precision Floating Point Multiplier, Proc. of 2003 IEEE ISSCC, February, 2003
		5.	Dobberpuhl et al., A 200-MHz 64-b Dual-Issue CMOS Microprocessor, IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992
		6.	Lin, Reconfigurable Parallel Inner Product Processor Architectures, IEEE T LSI, Vol. 9, No. 2. April 2001, pp. 261-272
		7.	Lin et al., An Extra-Regular, Compact, Low-Power Multiplier Design Using Triple-Expansion Schemes and Borrow Parallel Counter Circuits, in Proc. of Workshop on Complexity-Effective Design (WCED, ISCA), Held in conjunction with the 30th Intl. Symposium on Computer Architectures, San Diego, CA, June 2003
		8.	Lin, Low-Power High-Performance Non-Binary CMOS Arithmetic Circuits, in Proc. of 2000 IEEE Workshop on SiGNAL PROCESSING SYSTEMS (SiPS), Lafayette, Louisiana, October, 2000, pp. 477-486
		9.	Lin et al., Novel Design And Verification Of A 16 X 16-B Self-Repairable Reconfigurable Inner Product Processor, in Proc. of 12th Great Lakes Symposium on VLSI, NYC, April, 2002

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.